Amendments to the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Claims 1-26 (Cancelled).

27. (Original) A method of forming a dynamic random access memory (DRAM) comprising:

forming a plurality of conductive plugs received over substrate node locations over which storage capacitors are to be formed within a memory array area; and

after the forming of the plugs, removing insulative material over and exposing conductive material of conductive lines which are formed within a peripheral area outward of the memory array area, said exposing being a first-in-time exposure of conductive material of the conductive lines in the peripheral area after provision of said insulative material thereover.

28. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material, forming capacitor container openings within a second insulative material over conductive lines within the memory array area.

29. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material, contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area.

30. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material:

contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area; and

forming a capacitor electrode layer within the capacitor container openings and the contact openings.

31. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material:

contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area; and

forming a pair of capacitor electrode layers and an intervening dielectric region therebetween within the capacitor container openings and the contact openings.

32. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material:

contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area;

forming a capacitor electrode layer within the capacitor container openings and the contact openings; and

removing the capacitor electrode layer from within the contact openings and not from within the capacitor container openings.

33. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and further comprising prior to the removing of the first insulative material:

contemporaneously forming both capacitor container openings within a second insulative material over conductive lines within the memory array area, and contact openings within the second insulative material over the conductive lines within the peripheral area;

forming a capacitor electrode layer within the capacitor container openings; and

wherein the removing of the first insulative material comprises using an etch chemistry effective to remove both the first insulative material and selected portions of the capacitor electrode layer over the memory array.

34. (Original) The method of claim 27, wherein the forming of the plurality of conductive plugs comprises forming conductive material over the insulative material over the conductive lines within the peripheral area.

35. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and wherein:

the forming of the plurality of conductive plugs comprises forming conductive material over the first insulative material over the conductive lines within the peripheral area, and further comprising prior to the removing of the first insulative material, forming capacitor container openings over and exposing conductive plug portions within the memory array.

36. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and wherein:

the forming of the plurality of conductive plugs comprises forming conductive material over the first insulative material over the conductive lines within the peripheral area, and further comprising prior to the removing of the first insulative material, forming both capacitor container openings over and exposing conductive plug portions within the memory array, and contact openings over conductive lines within the peripheral area and exposing conductive material portions over the first insulative material.

37. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and wherein:

the forming of the plurality of conductive plugs comprises forming conductive material over the first insulative material over the conductive lines within the peripheral area, and further comprising prior to the removing of the first insulative material, forming both capacitor container openings over and exposing conductive plug portions within the memory array, and contact openings over conductive lines within the peripheral area and exposing conductive material portions over the first insulative material; and

forming a capacitor electrode layer within the capacitor container openings and the contact openings.

38. (Original) The method of claim 27, wherein the insulative material comprises a first insulative material, and wherein:

the forming of the plurality of conductive plugs comprises forming conductive material over the first insulative material over the conductive lines within the peripheral area, and further comprising prior to the removing of the first insulative material, forming capacitor container openings over and exposing conductive plug portions within the memory array; and

wherein the removing of the first insulative material comprises using an etch chemistry effective to remove both conductive material portions over the first insulative material and the first insulative material.

39. (Original) A method of forming a dynamic random access memory (DRAM) comprising:

forming a plurality of conductive plugs received over substrate node locations over which storage capacitors are to be formed within a memory array area; and

after the forming of the plugs, removing substantial portions of individual conductive line insulative caps over and exposing conductive material of conductive lines which are formed within a peripheral area outward of the memory array area.

40. (Original) The method of claim 39 further comprising after the forming of the plurality of conductive plugs:

forming an insulative material layer over the substrate; and

forming a plurality of openings received within the insulative material layer, some of the openings comprising capacitor container openings within which storage capacitors are to be formed, other of the openings comprising first contact openings formed over the insulative caps of the conductive lines within the peripheral area.

41. (Original) The method of claim 39 further comprising after the forming of the plurality of conductive plugs:

forming an insulative material layer over the substrate;

forming a plurality of openings received within the insulative material layer, some of the openings comprising capacitor container openings within which storage capacitors are to be formed, other of the openings comprising first contact openings formed over the insulative caps of the conductive lines within the peripheral area; and

forming a capacitor electrode layer within the capacitor container openings and the first contact openings.

42. (Original) The method of claim 39 further comprising after the forming of the plurality of conductive plugs:

forming an insulative material layer over the substrate;

forming a plurality of openings received within the insulative material layer, some of the openings comprising capacitor container openings within which storage capacitors are to be formed, other of the openings comprising first contact openings formed over the insulative caps of the conductive lines within the peripheral area;

forming a pair of capacitor electrode layers within the capacitor container openings and the first contact openings;

forming a patterned masking layer over the capacitor container openings; and

removing unmasked portions of the pair of capacitor electrode layers.

43. (Original) The method of claim 39 further comprising after the forming of the plurality of conductive plugs:

forming an insulative material layer over the substrate;

forming a plurality of openings received within the insulative material layer, some of the openings comprising capacitor container openings within which storage capacitors are to be formed, other of the openings comprising first contact openings formed over the insulative caps of the conductive lines within the peripheral area;

forming a pair of capacitor electrode layers within the capacitor container openings and the first contact openings;

forming a patterned masking layer over the capacitor container openings; and

removing unmasked portions of the pair of capacitor electrode layers, and wherein the removing of the substantial portions of the individual conductive line insulative caps comprises removing said portions with the patterned masking layer in place.

44. (Original) A method of forming a dynamic random access memory (DRAM) comprising:

forming a plurality of conductive lines over a substrate having a memory array area and a peripheral area outward of the memory array area;

forming conductive material over the substrate comprising:

conductive plugs received over substrate node locations over which storage capacitors are to be formed within the memory array area, and

conductive material received over portions of some of the conductive lines within the peripheral area;

forming openings through an insulative material and exposing the conductive plugs within the memory array area and the conductive material within the peripheral area;

forming a storage capacitor electrode layer within the openings; and

removing portions of the storage capacitor electrode layer within the memory array area and peripheral area sufficient to form a storage capacitor electrode within the memory array and entirely remove the storage capacitor electrode layer from within the peripheral area and outwardly expose conductive portions of conductive lines within the peripheral area.

45. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a cell plate layer within the openings.

46. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a cell plate layer within the openings, and

wherein the removing of the storage capacitor electrode layer comprises doing so in a common masking step.

47. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a cell plate layer within the openings, and wherein the removing of the storage capacitor electrode layer comprises doing so in a common etching step.

48. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a storage node layer within the openings.

49. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a storage node layer within the openings, and wherein the removing of the storage capacitor electrode layer comprises doing so in multiple removing steps.